



# Companion IP-Cores

DDR2 Memory controller • Memory Arbiter • UDP control Manager

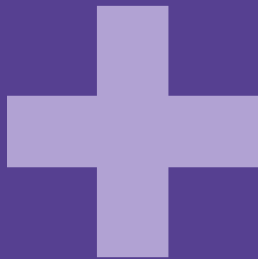


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In order to offer the most compact and complete solutions to customers, intoPIX proposes companion IP-Cores that have been especially designed to ease the integration of our JPEG 2000 encoders and decoders into your platform, speeding up time-to-market.

By completing your JPEG 2000 solutions with our companion IP-Cores, you will benefit from intoPIX's know-how for all your solutions.



**THE intoPIX PLUS**

- Ease JPEG 2000 integration
- Reduced FPGA footprint
- Flexible architecture
- Field upgradeable
- Customizable.



■ **Companion IP-Cores**

**IPX-DDR2:  
Memory Controller**

**GENERAL DESCRIPTION**

The IPX-DDR2 core is a DDR2 memory controller for Xilinx Virtex-4 and for Virtex-5 devices running up to 266 MHz and width bus width of up to 64 bits. This intoPIX core reduces the number of logic resources and improves the latency of row accesses. The DDR2 Memory controller guarantees efficient DDR2 access to the JPEG 2000 IP-cores and is fully compatible with all the families of intoPIX JPEG 2000 IP-cores.

The user interface is a bus of up to 256-bit width running at up to 133 MHz. The maximum peak rate transfer is  $64 \times 2 \times 266 \approx 34$  Gbit/s. The physical bus width is selectable between 8, 16, 32 and 64 bits, and the user interface is also selectable between 32, 64, 128 or 256 bit.

**KEY FEATURES**

**Configurable data memory width**

**Continuous random data accesses within the same row**

**Reduced footprint. Area is linear with respect to the data memory width**

**High operating frequency supported**

**Efficient integration with memory arbiter cores, including IPX-MA (Memory Arbiter)**

**RESOURCES**

	Virtex-4	Virtex-5
<b>Slices</b> (for a 32-bit wide physical data-bus; user data bus of 128-bit)	850	850
<b>RAMBs</b>	0	0
<b>DSPs</b>	0	0
<b>Frequency</b> (533 Mbps per data bit)	Up to 266 Mhz	Up to 266 Mhz



## IPX-MA: Memory Arbiter

### GENERAL DESCRIPTION

This IP-core is a 4-port arbiter - each port with the same width (32, 64, 128 or 256) - running up to 133 MHz. The block enables the external memory to be shared between different processes e.g. Frame buffers, Watermarking, PCI-Express buffers,...

The arbiter schedules the order in which requests access memory.

### RESOURCES

	Virtex-4	Virtex-5
<b>Slices</b>	200	150
<b>RAMBs</b>	0	0
<b>DSPs</b>	0	0
<b>Frequency</b>	Up to 125 MHz	Up to 133 MHz

### KEY FEATURES

High memory efficiency

Predictable

Fast

Fair

Flexible

## IPX-UDP: UDP Protocol Manager

### GENERAL DESCRIPTION

The IPX-UDP receives UDP packets (including video/audio assets) on a gigabit Ethernet link.

The MAC controller is based on the Tri-Mode MAC controller that is hard-coded within the Virtex-5 SXT or LXT technology.

intoPIX configures the MAC controller with a specific MAC address read from a dedicated register and also sets up the external PHY chip.

The selected protocol (SGMII, GMII or RGMII), the exact chip reference and the corresponding user manual must be provided by the customer. To speed up the development, intoPIX recommends SGMII protocol.

The protocol handler will manage the user UDP protocol. This handler is in charge of:

- receiving video/audio packets,
- verifying the integrity with IP and UDP checksum and Ethernet CRC,
- sending a response packet back for every n packets received.

If a packet is missing or corrupted, the UDP handler will reject all subsequent packets while waiting for a correct retransmission of its related n packet group.

### RESOURCES

	Virtex-4	Virtex-5
<b>Rocket IOs</b>	2	2
<b>Slices</b>	2000	1200
<b>RAMBs</b>	16 RAMBs (for 1500 bytes Ethernet Frames)	8 RAMBs
<b>DSPs</b>	0	0
<b>Frequency</b>	125 MHz	125 MHz
<b>PHY componnt</b>	Marvell 88E1111 (with SGMII protocol) or any other compatible chip	

### KEY FEATURES

Reduced footprint

Supports Gigabit Ethernet

Highly integrated





## ■ Companion IP-Cores Matrix



		Xilinx Virtex 4 - FPGA Reference				Xilinx Virtex 5 - FPGA Reference					
		Slices	RAMBs	DSPs	Frequency	Slices	RAMBs	DSPs	Frequency		
Companion IP-cores	<b>IPX-DDR2</b>	Memory Controller DDR2		850	0	0	266	510	0	0	266
	<b>IPX-MA</b>	Memory arbiter		200	0	0	125	150	0	0	133
	<b>IPX-UDP</b>	UDP Protocol Manager		2000	16	0	125	1200	8	0	125

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## ■ About intoPIX

intoPIX develops and commercializes high-end image processing and security tools in large data streams with high intrinsic value. The applications are aimed especially at pictures having demanding requirements in quality, security and authoring rights. Based in Louvain-la-Neuve (Belgium), intoPIX was established in 2005, quickly becoming the international reference for hardware JPEG 2000 coding solutions.

intoPIX's world leading expertise includes FPGA and software engineering, JPEG 2000 image compression and symmetric-asymmetric security.

intoPIX's solutions are dedicated to the Digital Cinema, Digital Archiving, Camera, Field Recorder, Video Server, Broadcast contribution and Wireless transmission areas.

intoPIX efficiently combines on-chip hardware and software operations for an optimal co-design repartition of the coding blocks, it also provides a unique post-deployment core renewability for field upgrade and update. intoPIX IP-cores are especially targeting image and video applications.

### More information

Ask intoPIX how to bring your JPEG 2000 requirements to life!

Email : [sales@intopix.com](mailto:sales@intopix.com)

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