

IPX-JP4K

decoder module

JPEG 2000 4K DECODER MODULE

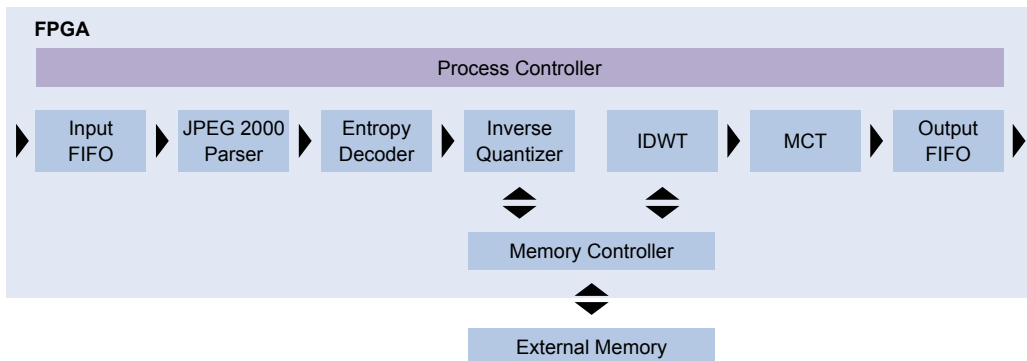
The IPX-JP4K module is an FPGA based JPEG 2000 decoder designed to meet the needs of high data rate processing for such demanding applications as Digital Cinema playback system and large picture and document archive access.

The FPGA flexibility enables custom combination of IPX-JP4K core with security IPX-AES and watermarking cores, to meet specific application requirements.

Efficiently combining on-chip hardware and software operations for an optimal co-design repartition of the decoding blocks, the IPX-JP4K also provides a unique post-deployment core renewability for field upgrade and update.

IPX-JP4K supports input bitrate up to 500 Mbps and can be adapted to provide any picture size (up to 4096 x 2160). The decoder is capable to output up to 24 and 96 frames per second (FPS) for 4K and 2K resolutions respectively, and an output bitrate up to 7,6 Gbit/s.

The IPX-JP4K can output in RGB, YUV or XYZ component formats and provides easy input and output data interfacing through a simple synchronous FIFO.



JPEG 2000 PARSER

The JPEG 2000 parser analyses the main and tile-part headers of the JPEG 2000 codestream and sends the compressed bit-stream to the entropy decoder.

ENTROPY DECODER

The reconstruction of each wavelet sub-band divided into several code-blocks is achieved by two blocks: the Context Modeller and the Arithmetic Decoder.

The Context Modeller successively decodes each bit-plane of the codeblock by sending information describing the neighbourhood of each bit to the Arithmetic Decoder. With this information, the Arithmetic Decoder decodes the bit-stream.

INVERSE QUANTIZER

The coefficients of the wavelet subbands are inverse quantized. The quantization steps are defined in the main header of the JPEG 2000 file and can be different for each subband.

EXTERNAL MEMORY

A frame memory buffer is used at the Inverse Quantizer output and enables an efficient IDWT processing. This buffer, containing one DDR2-SDRAM external memory, always keeps at least one valid frame that can be repeated when convenient. The required DDR2-SDRAM type is a 2 Gbit memory (128 Meg x 16 x 266 MHz).

INVERSE DISCRETE WAVELET TRANSFORM (IDWT)

A bidimensional wavelet recomposition of the subbands is achieved. Two filter banks, with a 18-bit fixed point precision, may be used: either the Le Gall (5/3) filter bank prescribed for lossless encoding or either the more complex Daubechies (9/7) filter bank for lossy encoding.

■ Affordable single chip solution

■ Field upgradeable

■ Customizable

■ Configurable to any frame rate or size

■ High bit-rate capable



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MULTIPLE COMPONENT TRANSFORMATION (MCT)

In the JPEG 2000 standard, in order to improve compression efficiency, multiple component transformations can be used. Depending on the wavelet filters used, different transformations are defined. The reversible transform (RCT) is used with the 5/3 filter, and the irreversible transform (ICT) with the 9/7 filter. Both transformations are implemented with a 18-bit fixed point precision.

ERROR HANDLING

The decoder is designed to detect errors in the input data. This detection is achieved at two levels:

- **JPEG 2000 header**

Codestream characteristics such as image size and bits per components are checked. The coherence of the J2K headers with the specifications given by the decoder controller is analysed.

- **JPEG 2000 packet headers and compressed bit-stream**

Packet headers are analysed to verify the coherence of tag trees, number of bit-planes, code-block compressed bit-stream length, ...

When an error is detected, specific error codes are sent to the device managing the decoder. In the case of a corrupted frame codestream, the decoder can try to decode the next frame. This can be repeated until a correct frame is encountered. If no frame can be decoded during the elapsed time determined by the frame rate, the previous correctly decoded frame is sent to the output to prevent display artifact.

PROCESS CONTROL

Taking advantage of the JPEG 2000 intra-frame coding, the decoder controller can manage the stream at the frame accuracy. When there is no data to decode at its input, the decoder can loop on the latest decoded frame, output a black frame or stop to output frames.

By controlling the input stream and the output options, the decoder controller can manage pause, step by step, slowmotion, fast forward and rewind, and random access.

INTERFACES

The input receives data by 32-bit bursts, in Little-Endian representations. A burst of two pixels (in RGB, YUV or XYZ) is output. The output clock depends on the sequence frame rate and picture size.

DC requirement check list

- ✓ **JPEG 2000 (ISO/IEC 15444-1)**
- ✓ **250 Mbits/sec input**
- ✓ **2K / 24 FPS**
- ✓ **2K / 48 FPS**
- ✓ **4K / 24 FPS**
- ✓ **12-bit color depth**
- ✓ **X-Y-Z color space**
- ✓ **9/7 wavelet filter**
- ✓ **18-bit fixed point IDWT**
- ✓ **18-bit fixed point ICT**

| | |
|---------------------------------|---|
| Image Coding Format | JPEG 2000 : ISO/IEC 15444-1 |
| Wavelet Transform Filter | 5/3 and 9/7 filters 18-bit fixed point precision |
| Tiles | Single or multiple tiles |
| Quality Layer | Single quality layer (Multiple quality layers optional) |
| Resolutions | Up to 7 resolutions |
| Code Block size | 32 x 32 pixels |
| Code Block coding style | Standard JPEG 2000 options |
| Input data-rate | Up to 500 Mbit/s |
| Image size | Up to 4096 x 2160 pixels |
| Frame-rate | 24/48/96 FPS for 2K and 24 FPS for 4K |
| Output throughput | Up to 7,6 Gbit/s |
| Component transform | RCT and ICT 18-bit fixed point precision |
| Color output format | RGB, XYZ and YUV |
| Color Depth | Up to 12 bits per component |
| Recommended FPGA | Virtex-4 FX60-10 |



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