

# IPX-JPHD

JPEG 2000 encoder/decoder

l e a d i n g t h e w a y

## ■ IPX-JPHD IP Core Family

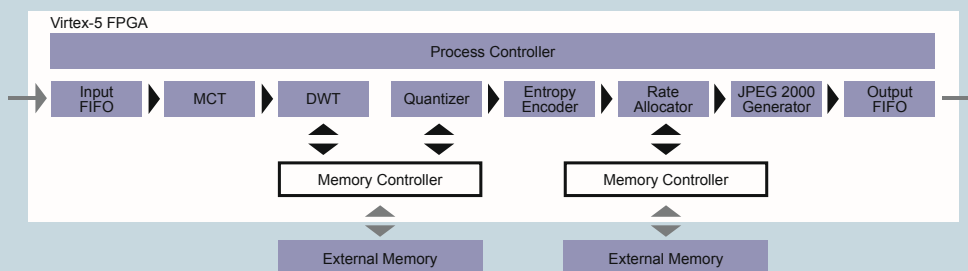
The IPX-JPHD is a high quality and cost effective family of FPGA based JPEG 2000 encoders and decoders designed to meet the requirements of high data rate processing in broadcast Acquisition, Storage and Contribution.

Based on a single chip, the exceptionally flexible IPX-JPHD family supports variable compression ratio's up to Lossless and can be adapted to any image resolution up to HD (1920 x 1080).

The powerful IPX-JPHD modules also provide a compact and reliable solution to broadcasters need for Multi-channel operation through a unique single chip design that enables up to four HD channels to be streamed simultaneously at a total frame rate of 120fps.

Purpose designed for the Xilinx® FPGA the IPX-JPHD family is a no compromise solution that takes full advantage of the benefits of the state-of-the-art Virtex-5™ platform including easy connection to HD-SDI, SDI, SDTI, ASI, PCI-Express® and Gigabit Ethernet broadcast and system interfaces.

## ■ IPX-JPHD Encoder Module



### MULTIPLE COMPONENT TRANSFORMATION (MCT)

To improve compression efficiency multiple component transformations may be used and, depending on the wavelet filters used, different transformations defined. The reversible Lossless transform (RCT) is used with the 5/3 filter, and the irreversible transform (ICT) with the 9/7 filter. Both transformations are implemented with 18-bit fixed point precision.

### DISCRETE WAVELET TRANSFORM (DWT)

A bi-dimensional wavelet decomposition of the sub-bands is performed with either the Le Gall (5/3) filter bank (prescribed for Lossless encoding) or the Daubechies (9/7) filter bank for Lossy encoding being used with 18-bit fixed point precision.

### QUANTIZER

The coefficients of the wavelet sub-bands are quantized. The quantization steps are defined by the user and can be different for each sub-band.

### ENTROPY ENCODER

Each wavelet sub-band is divided into several code-blocks and encoded using an Entropy Encoder. The encoder is divided into two blocks: the Context Modeler and the Arithmetic Encoder. The Context Modeler successively encodes each bit-plane of the code-block by sending information describing the neighborhood of each bit to the Arithmetic Encoder. With this information the Arithmetic Encoder encodes each bit in order to generate the compressed bit-stream.

### RATE ALLOCATOR

In order to maximize image quality within the bitrate limit boundaries fixed by the user, the Rate Allocator selects the information encoded by the Entropy Encoder that will be finally included in the stream.

### JPEG 2000 GENERATOR

The JPEG 2000 Generator is responsible for generating the final code-stream so as to provide a fully compliant JPEG 2000 image.

■ Ultra dense  
FPGA solution

■ Single chip

■ Virtex-5™  
technology

■ Compatible  
with standard  
Broadcast I/O  
interfaces

■ Multi-stream  
capabilities

■ Configurable  
image size  
and frame rate

■ Up to 120 fps

■ Variable  
compression  
up to Lossless



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**EXTERNAL MEMORIES**

A first memory buffer is used to provide the most efficient DWT processing. This buffer, containing one DDR2-SDRAM external memory, enables the IPX-JPHD to provide a buffer of at least one frame. A second memory buffer is then provided to efficiently compute the rate allocation. This buffer is also based on one DDR2-SDRAM memory. The DDR2-SDRAM types included will depend on the user specification and required product solution.

**INTERFACES**

Input and output interfaces are based on FIFO protocols, and a burst of two pixels (in RGB or YUV) required at the input interface.

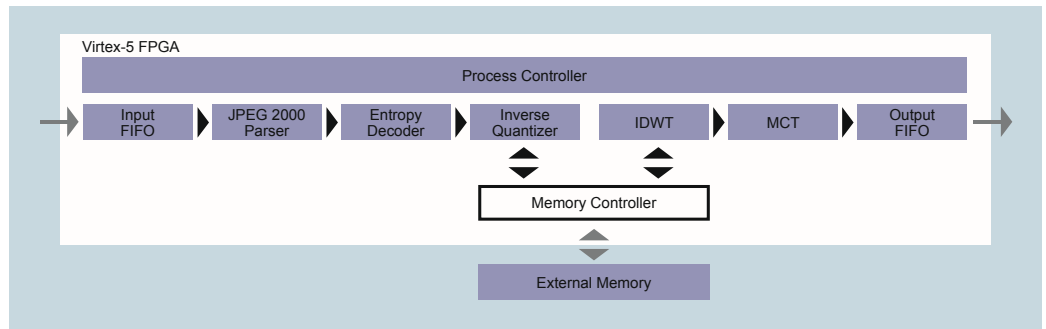
**PROCESS CONTROLLER**

Taking full advantage of JPEG 2000 intra-frame coding the IPX-JPHD Process Controller accurately manages the frame stream. When there is no video to encode the processor will continue to provide the latest encoded frame, or stop outputting compressed data according to the user command. This process also configures the different JPEG 2000 options for the full encoding chain.

**IPX-JPHD Decoder Module**

The IPX-JPHD Decoder module also takes full advantage of the flexibility, compactness and interfacing capabilities of the Xilinx Virtex-5 technology.

The dataflow of IPX-JPHD Decoder illustrated below largely replicates the IPX-JPHD Encoder with the exception of the Parser and Error Handling.



**JPEG 2000 PARSER**

The JPEG 2000 Parser analyses the main and tile-part headers of the JPEG 2000 codestream and sends the compressed bit-stream to the Entropy Decoder.

**ERROR HANDLING**

The decoder is designed to detect errors in the input data and detection achieved at the main header, packet headers, and at the coherence of tag trees.

**IPX-JPHD Applications**

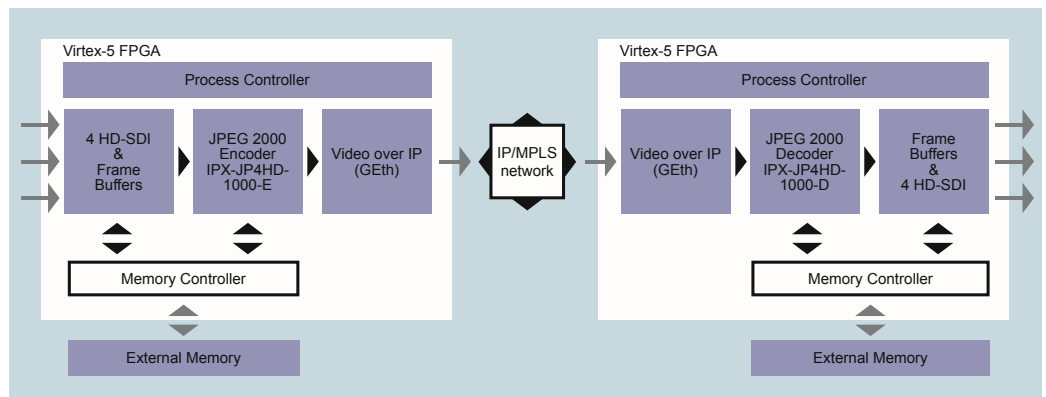
**CONTRIBUTION**

IPX-JPHD is ideally suited to real-time Contribution requiring the transport of live video material between different locations, including content exchanges and live events coverage between studios or stadium and production house, with the minimum transport delay.

of high quality content is easily managed through the inherent support of all relevant physical interfaces in Virtex-5.

IPX-JPHD simply and efficiently meets the critical requirement for high-quality and error-resilient encoding, plus the compression of multiple video channels into a single stream - while the distribution

As the above illustration shows four HD-SDI channels and one Gigabit Ethernet using the IPX-JP4HD-1000 encoding/decoding cores is all that is needed for the highest quality cost effective solution to the most demanding contribution requirement.





**STORAGE**

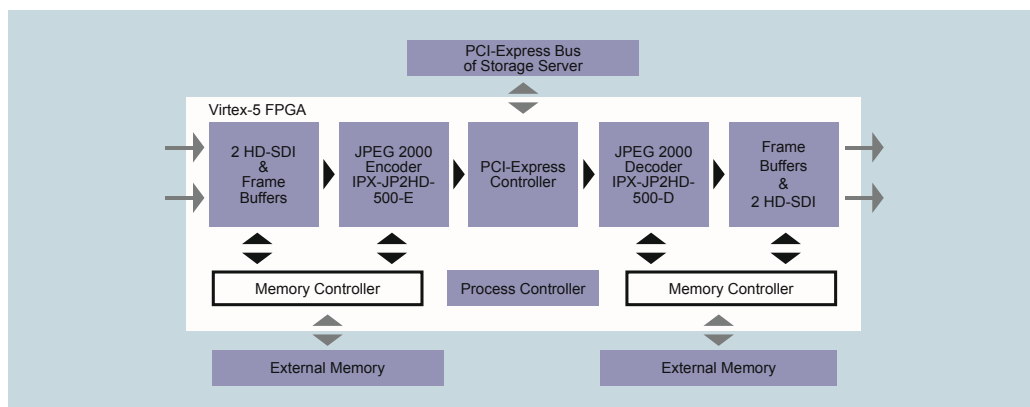
As efficient video storage becomes increasingly important JPEG 2000 compression offers an ideal solution.

While servers must be capable of ingesting and storing multiple video streams in real time it is also essential for editing that storage systems use the appropriate Lossy compression to avoid the progressive reduction of quality through successive compression and decompression operations.

Unlike MPEG compression-decompression (which introduces additional degradation at each step) a

JPEG 2000 file maintains the image quality corresponding to the highest compression rate of the chain.

The following diagram illustrates a video storage application based on an intoPIX JPEG 2000 codec composed of IPX-JP2HD-500-E and IPX-JP2HD-500-D cores running in a single FPGA, with the Virtex-5 providing direct interface to the PCI-Express input.



**IPX-JPHD Product Range**

The following table is a summary of the IPX-JPHD range showing the FPGA requirement for different cores and the required DDR2-SD RAM.

All listed devices have enough free resources to implement video I/O interfaces, system interfaces or security IP's.

PRODUCT NAME	FPGA	DDR2-SDRAM MODELS
IPX-JP1*HD-250**-E***	XC5VSX50T-1	64 Meg x 16 x 266 MHz
IPX-JP1HD-250-D	XC5VSX50T-1	64 Meg x 16 x 266 MHz
IPX-JP2HD-500-E	XC5VLX85T-1	64 Meg x 32 x 266 MHz
IPX-JP2HD-500-D	XC5VSX50T-1	64 Meg x 32 x 266 MHz
IPX-JP4HD-1000-E	XC5VSX95T-1	64 Meg x 64 x 266 MHz
IPX-JP4HD-1000-D	XC5VSX95T-1	64 Meg x 64 x 266 MHz
IPX-JP1HD-L-E	XC5VLX85T-1	64 Meg x 16 x 266 MHz
IPX-JP1HD-L-D	XC5VLX85T-1	64 Meg x 16 x 266 MHz

**PRODUCT CODES**

**\* Multiple Channel options**

Each IPX JPHD Encoder and Decoder is available in 1, 2 and 4 channel configurations

**\*\* Speed**

250 - Up to 250 Mbps • 500 - Up to 500 Mbps • 1000 - Up to 1000 Mbps • L - Lossless

**\*\*\* Type**

E denotes Encoder and D a Decoder module





# IPX-JPHD

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### General Specifications IPX-JPHD

IMAGE CODING FORMAT	JPEG 2000 ISO/IEC 15444-1
<b>Wavelet transform filter</b>	<ul style="list-style-type: none"> <li>• 5/3 and 9/7 filters, 18-bit fixed point precision</li> <li>• 5/3 for Lossless compression</li> <li>• 9/7 for Lossy compression</li> </ul>
<b>Component transform</b>	<ul style="list-style-type: none"> <li>• RCT and ICT 18-bit fixed point precision</li> <li>• RCT for Lossless compression</li> <li>• ICT for Lossy compression</li> </ul>
<b>Wavelet decompositions</b>	<ul style="list-style-type: none"> <li>• Up to 6 decompositions</li> </ul>
<b>Tiles</b>	<ul style="list-style-type: none"> <li>• Single tile (multiple tiles are optional)</li> </ul>
<b>Quality layer</b>	<ul style="list-style-type: none"> <li>• Single quality layer</li> </ul>
<b>Code block size</b>	<ul style="list-style-type: none"> <li>• 32 x 32 pixels (other sizes are optional)</li> </ul>
<b>Code block coding style</b>	<ul style="list-style-type: none"> <li>• Standard JPEG 2000 options</li> </ul>
<b>Compressed data rate</b>	<ul style="list-style-type: none"> <li>• Up to Lossless</li> </ul>
<b>Image resolution</b>	<ul style="list-style-type: none"> <li>• Up to 1920 x 1080 /channel</li> </ul>
<b>Frame rate</b>	<ul style="list-style-type: none"> <li>• Up to 120fps total @ HD resolution</li> </ul>
<b>Color format</b>	<ul style="list-style-type: none"> <li>• RGB or YUV</li> </ul>
<b>Chroma subsampling</b>	<ul style="list-style-type: none"> <li>• 4:4:4 or 4:2:2</li> </ul>
<b>Color depth</b>	<ul style="list-style-type: none"> <li>• Up to 12 bits per component</li> </ul>
<b>Progression order</b>	<ul style="list-style-type: none"> <li>• CPRL</li> </ul>
<b>Precinct size</b>	<ul style="list-style-type: none"> <li>• 128x128 for the smallest LL subband</li> <li>• 256x256 for other subbands</li> </ul>

### PHYSICAL INTERFACES

All relevant physical interfaces are supported:  
HD-SDI, SDTI, ASI, PCI Express®, Endpoint, Gigabit Ethernet.

### FRAMES PER SECOND

The table below examples the maximum frame rate achievable at 4:4:4 resolution at 12 bits depending on the multi-channel option used. Custom requirements are available on request.

IPX-JPHD PRODUCT	NUMBER OF CHANNELS	RESOLUTION 4:4:4, 12 BITS	FRAME RATE (PROGRESSIVE)
IPX-JP1HD	1	1920 x 1080	30 fps/ch
IPX-JP2HD	2	1920 x 1080	30 fps/ch
IPX-JP2HD	1	1920 x 1080	60 fps/ch
IPX-JP4HD	4	1920 x 1080	30 fps/ch
IPX-JP4HD	2	1920 x 1080	60 fps/ch



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