The disruptive visually lossless light video compression, extremely tiny in FPGA

A TECHNOLOGY SERVING THE GLOBAL AV INDUSTRY

TICO is a new visually lossless compression specifically designed for the industry. This revolutionary technology is extremely tiny in FPGA fitting the smallest Xilinx Artix-7 and Spartan-6 devices, robust for real-time operation with no latency.

Up to now, image and video are sent or stored uncompressed into many displays and systems such as cameras, videos servers or recorders. TICO is a smart upgrade path to manage higher resolutions (4K, 8K …) and frame rates while assuring visual quality, keeping power and bandwidth at a reasonable budget and reducing significantly the complexity and cost of the system.

Technology benefits

- Visually Lossless quality:
  - Up to 4:1
  - Robust over multiple encoding generations
  - Math. lossless at lower compression ratio

- Fixed latency: down to microseconds
  - Selectable from 2 to x pixel lines

- Very low FPGA resource requirement:
  - No external memory - only compressed line buffer
  - Low power consumption

- Powerful, real-time or faster than real-time in CPU

- Compatible with different resolutions, from mobile, HD to 4K/8K UHDTV, via multiple usual transport schemes

- Designed to be a standard for industry-wide support: TICO compression technology is available on multiple software and hardware technologies code, hardware IP-cores and software libraries are available

- SMPTE RDD35 Compliant:
  - TICO over IP (SMPTE2022 5/6 & RTP) and over SDI infrastructures (4K over 3G-SDI)
Typical applications from HD to Ultra HD

- Video over IP systems (SMPTE2022, VSF TR03, AVB, ...)
- Video servers, routers and switches
- Cameras (high-res, real-time or high speed)
- Video monitors and displays
- Frame grabbers and video capture devices
- Cable extenders
- UHD/4K over 3G-SDI, over 10GbE
- UHD/8K over 12G-SDI, over 25GbE/40GbE, ...
- Video recorders & players
- (...)

TICO is a smart solution to

- Support higher data stream using existing systems & infrastructures (HD/4K/8K/HFR)
- Increase the number of streams or the stream resolution
- Reduce the internal video bandwidth (and power!)
- Cost effectively increase video buffer and storage capacity
- Reduce the number of lanes needed to transport a stream at a display interface or at an image sensor to save power, cost or both

FPGA implementation

- Color modes: 4:0:0, 4:2:0, 4:2:2 and 4:4:4:4, RGB, YCbCr, XYZ, RAW bayer
- Bit Depth: 8, 10 or 12
- Resolutions: Any up to 8K (8192 x 8192)
- Frame Rates: Any (depending on intoPIX IP-core configuration)

FPGA

- (Sub) Intra-frame
- Real-time operation guaranteed (no overflow or underflow)
- Fixed latency
  - Selectable from 3 lines up to 11 at decoder, from 6 lines up to 18 at encoder, lowest latency is with Profile 1
- Adjustable rate for Lossy/Visually lossless (up to 4:1) / Math. lossless (1.2:1 to 1.8:1)
- CBR (constant bit rate) operation (optional capped VBR mode)
- TICO Profile 1 & 2 support
- SMPTE RDD35 compliant
- Embedded x2 downscaler option in Decoder

FPGA IP-Cores releases

<table>
<thead>
<tr>
<th>Reference IP-cores (Profile 1 or 2, -Enc or -Dec)</th>
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<th>Max FPS</th>
<th>Color Sampling</th>
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- Video formats
- Target Xilinx
  - Low end FPGAs: Xilinx Spartan-6 & Artix-7
  - High end FPGAs: Xilinx Kintex-7, Virtex-7 & Ultrascale

Xilinx FPGA

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*Available in pre-order only.

Contact intoPIX for your own custom IP-core configuration

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