The disruptive **lossless quality video compression**, extremely tiny in FPGA

A TECHNOLOGY SERVING THE GLOBAL AV INDUSTRY

This revolutionary technology is extremely tiny in FPGAs fitting the smallest Intel FPGA Cyclone devices, robust for real-time operation with no latency.

Up to now, image and video are sent or stored uncompressed into many displays and systems such as cameras, videos servers, or recorders. TICO is a smart upgrade path to manage higher resolutions (4K, 8K, …) and frame rates while assuring visual quality, keeping power and bandwidth at a reasonable budget, and significantly reducing the complexity and cost of the system.

**Technology benefits**

- **Visually lossless quality:**  
  - 2:1 to 8:1  
  - Robust over multiple encoding generations  
  - Math. lossless at lower compression ratio

- **Fixed latency:** down to microseconds  
  - Selectable from 2 to x pixel lines

- **Very low FPGA resource requirement:**  
  - No external memory - only compressed line buffer  
  - Low power consumption

- **Powerful, real-time or faster than real-time in CPU**

- **Compatible with different resolutions, from mobile, HD to 4K/8K UHDTV, via multiple usual transport schemes**

- **Designed to be a standard for industry-wide support:** TICO compression technology is available on multiple software and hardware technologies

- **SMPTE RDD35 Compliant:**  
  TICO over IP (SMPTE 2022 5/6 & RTP for SMPTE 2110) and over SDI infrastructures (4K over 3G-SDI)
**FPGA IP-Cores releases**

<table>
<thead>
<tr>
<th>Reference IP-Cores (Profile 1 or 2, -Enc or -Dec)</th>
<th>Max Resolution</th>
<th>Max FPS</th>
<th>Color Sampling</th>
<th>Bit Depth</th>
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<tbody>
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<td>IPX-TICO-HD-60-422</td>
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* Available in pre-order only.

**FPGA IP-Cores releases**

**Video formats**

**Target Intel FPGA**

**Low end FPGAs Intel Cyclone V & Arria V**

**High-end FPGAs Intel Arria V G6, Stratix V & Arria 10**

**Contact INTOPIX for your own custom IP-core configuration**

**HEADQUARTERS:** intoPIX SA  
 Rue Emile Francqui 9  
B-1435 Mont-Saint-Guibert - Belgium  
Tel.: +32 10 23 84 70  
sales@intopix.com

**CHINA:** sales.hypersilicon@intopix.com  
sales.waterstone@intopix.com

**INDIA:** sales.india@intopix.com

**ISRAEL:** sales.israel@intopix.com

**JAPAN:** sales.japan@intopix.com

**USA:** sales@intopix.com

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**FPGA Implementation**

**Image features**

**Compression** (Latency, Quality, Rate Control)

- (Sub) Intra-frame
- Real-time operation guaranteed (no overflow or underflow)
- Fixed latency
  - Selectable from 3 lines up to 11 at decoder, from 5 lines up to 18 at encoder
  - Lowest latency is with Profile 1
- Adjustable rate for Lossy/Visually lossless (up to 4:1) / Math. lossless (1.2:1 to 1.8:1)
- CBR (constant bit rate) operation (optional capped VBR mode)
- Embedded x2 downsampler option in Decoder

**FPGA**

- Low cost implementation in any Intel FPGAs: very low FPGA logic and internal RAM usage
- Fit in the smallest Intel FPGA Cyclone V, Arria V, Stratix V & Arria 10 families
- Encoder and decoder have approximately the same complexity
- IP-core customizable per application, delivered within a HDK to speed up the integration
- Various pixel per clock implementations

**TICO is a smart solution to**

- Support higher data stream using existing systems & infrastructures (HD/4K/8K/HFR)
- Increase the number of streams or the stream resolution
- Reduce the internal video bandwidth (and power!)
- Cost effectively increase video buffer and storage capacity
- Reduce the number of lanes needed to transport a stream at a display interface or at an image sensor to save power, cost or both

**Typical applications from HD to Ultra HD**

- Video over IP systems (SMPTE 2022, SMPTE 2110, AVB, ...)
- Video servers, routers and switches
- Cameras (high-res, real-time or high speed)
- Video monitors and displays
- Frame grabbers and video capture devices
- Cable extenders
- UHD/4K over 3G-SDI, over 10GbE
- UHD/8K over 12G-SDI, over 25GbE/40GbE, ...
- Video recorders & players

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