The disruptive lossless quality video compression, extremely tiny in FPGA

A TECHNOLOGY SERVING THE GLOBAL AV INDUSTRY

This revolutionary technology is extremely tiny in FPGAs, fitting the smallest Xilinx Artix-7 and Spartan-6 devices, robust for real-time operation with no latency.

Up to now, image and video are sent or stored uncompressed into many displays and systems such as cameras, video servers or recorders. TICO is a smart upgrade path to manage higher resolutions (4K, 8K, …) and frame rates while assuring visual quality, keeping power and bandwidth at a reasonable budget, and significantly reducing the complexity and cost of the system.

Technology benefits

- Visually lossless quality:
  - 2:1 to 8:1
  - Robust over multiple encoding generations
  - Math. lossless at lower compression ratio

- Fixed latency: down to microseconds
  - Selectable from 2 to x pixel lines

- Very low FPGA resource requirement:
  - No external memory - only compressed line buffer
  - Low power consumption

- Powerful, real-time or faster than real-time in CPU

- Compatible with different resolutions, from mobile, HD to 4K/8K UHDTV, via multiple usual transport schemes

- Designed to be a standard for industry-wide support: TICO compression technology is available on multiple software and hardware technologies

- SMPTE RDD35 compliant:
  - TICO over IP (SMPTE 2022 5/6 & RTP for SMPTE 2110-22) and over SDI infrastructures (4K over 3G-SDI)

- Selected as the baseline of the new JPEG-XS standard
**Typical applications from HD to Ultra HD**

- Video over IP systems (SMPTE 2022, SMPTE 2110-22, …)
- Video servers, routers and switchers
- Cameras (high-res, real-time or high speed)
- Video monitors and displays
- Frame grabbers and video capture devices
- Cable extenders
- UHD/4K over 3G-SDI, over 10Gbe
- UHD/8K over 12G-SDI, over 25Gbe/40GbE, …
- Video recorders & players
- …

**TICO is a smart solution to**

- Support higher data streams using existing systems & infrastructures (HD/4K/8K/HFR)
- Increase the number of streams or the stream resolution
- Reduce the internal video bandwidth (and power !)
- Cost effectively increase video buffer and storage capacity
- Reduce the number of lanes needed to transport a stream at a display interface or at an image sensor to save power, cost or both

**FPGA implementation**

**Image features**

- Color modes: 4:0:0, 4:2:0, 4:2:2 and 4:4:4, RGB, YCbCr, XYZ, RAW bayer
- Bit Depth: 8, 10, 12, 14 & 16
- Resolutions Any up to 10K (10240 x 10240)
- Frame Rates: Any (depending on intoPIX IP-core configuration)

**Compression**

(Latency, Quality, Rate Control)

- (Sub) Intra-frame
- Real-time operation guaranteed (no overflow or underflow)
- Fixed latency
- Selectable from 3 lines up to 11 at decoder, from 6 lines up to 18 at encoder, lowest latency with Profile 1
- Adjustable rate for lossy/visually lossless (up to 4:1/math. lossless 1.2:1 to 1.8:1)
- CBR (constant bit rate) operation (optional capped VBR mode)
- TICO Profile 1 & 2 support
- SMPTE RDD35 compliant
- Embedded x2 downscaler option in decoder

**FPGA**

- Low cost implementation in any Xilinx FPGAs: very low FPGA logic and internal RAM usage
- Fits in the smallest Xilinx Spartan-6, Artix-7, Kintex-7 and Kintex Ultrascale
- Encoder and decoder have approximately the same complexity
- IP-core customizable per application, delivered within an HDK to speed up the integration
- Various pixel per clock implementations

**FPGA IP-Cores releases**

<table>
<thead>
<tr>
<th>Reference IP-cores</th>
<th>Max resolution</th>
<th>Max FPS</th>
<th>Color sampling</th>
<th>Bit depth</th>
</tr>
</thead>
<tbody>
<tr>
<td>(Profile 1 or 2, -Enc or -Dec)</td>
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<tr>
<td><strong>HDTV/2K</strong></td>
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<tr>
<td>IPX-TICO-HD-60-422</td>
<td>1920x1080</td>
<td>60</td>
<td>4:2:2</td>
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<tr>
<td>IPX-TICO-UHD4K-60-422</td>
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<td>4:2:2</td>
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<td>IPX-TICO-UHD4K-120-422</td>
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<td>8, 10, 12, 16</td>
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<td>IPX-TICO-UHD4K-120-444</td>
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<td><strong>UHDTV2/8K</strong></td>
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</tbody>
</table>

*Available in pre-order only.

**CONTACT INTOPIX FOR YOUR OWN CUSTOM IP-CORE CONFIGURATION**

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