



The disruptive lossless quality video compression, extremely tiny in FPGA

A TECHNOLOGY SERVING THE GLOBAL AV INDUSTRY

This revolutionary technology is extremely tiny in FPGAs, fitting the smallest Xilinx Artix-7 and Spartan-6 devices, robust for real-time operation with no latency.

Up to now, image and video are sent or stored uncompressed into many displays and systems such as cameras, videos servers or recorders. TICO is a smart upgrade path to manage higher resolutions (4K, 8K, ...) and frame rates while assuring visual quality, keeping power and bandwidth at a reasonable budget, and significantly reducing the complexity and cost of the system.



Take IMAGING to the NEXT LEVEL

|) TICO is a smart solution to b support higher data streams using existing systems & infrastructures (HD/4K/8K/HFR) Increase the number of streams or the stream resolution Reduce the internal video bandwidth (and power!) Cost effectively increase video buffer and storage capacity Reduce the number of lanes needed to transport a stream at a display interface or at an image sensor to save power, cost or both Color modes: 4:0:0, 4:2:0, 4:2:2 and 4:4:4, RGB, YCbCr, XYZ, RAW bayer Bit Depth: 8, 10, 12, 14 & 16 Resolutions Any une to 10K (10240 x 40240) |
|--|
| Resolutions Any up to TOK (TO240 x TO240) Frame Rates: Any (depending on intoPIX IP-core configuration) (Sub) Intra-frame Real-time operation guaranteed (no overflow or underflow) Fixed latency Selectable from 3 lines up to 11 at decoder, from 6 lines up to 18 at encoder, lowest latency with Profile 1 Adjustable rate for lossy/visually lossless (up to 4:1) /math. lossless (1.2:1 to 1.8:1) CBR (constant bit rate) operation (optional capped VBR mode) TICO Profile 1 & 2 support SMPTE RDD35 compliant Embedded x2 downscaler option in decoder |
| Low cost implementation in any Xilinx FPGAs: very low FPGA logic and internal RAM usage Fits in the smallest Xilinx Spartan-6, Artix-7, Kintex-7 and Kintex Ultrascale Encoder and decoder have approximately the same complexity IP-core customizable per application, delivered within an HDK to speed up the integration Various pixel per clock implementations |
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📶 FPGA IP-Cores releases

| | | Video formats | | | | Target Xilinx FPGA | |
|----------|--|----------------|---------|----------------|---------------|---|---|
| | Reference IP-cores (Profile 1 or 2, -Enc or -Dec) | Max resolution | Max FPS | Color sampling | Bit depth | Low-end FPGAs Xilinx Spartan-6 & Artix-7 | High end FPGAs Xilinx Kintex-7, Virtex-7 & Ultrascale |
| HDTV/2K | IPX-TICO-HD-60-422 | 1920x1080 | 60 | 4:2:2 | 10 | \checkmark | \checkmark |
| | IPX-TICO-HD-120-422 | 1920x1080 | 120 | 4:2:2 | 10 | ✓ | \checkmark |
| | IPX-TICO-HD-180-422 | 1920x1080 | 180 | 4:2:2 | 10 | ✓ | \checkmark |
| | IPX-TICO-HD-240-422 | 1920x1080 | 240 | 4:2:2 | 10 | \checkmark | \checkmark |
| | IPX-TICO-HD-360-422 | 1920x1080 | 360 | 4:2:2 | 10 | / | \checkmark |
| | IPX-TICO-HD-60-444 | 2048x1200 | 60 | 4:2:2 / 4:4:4 | 8, 10, 12, 16 | \checkmark | \checkmark |
| | IPX-TICO-HD-120-444 | 2048x1200 | 120 | 4:2:2 / 4:4:4 | 8, 10, 12, 16 | \checkmark | \checkmark |
| | IPX-TICO-HD-240-444 | 2048x1200 | 240 | 4:2:2 / 4:4:4 | 8, 10, 12, 16 | ✓ | \checkmark |
| uhdtv/4k | IPX-TICO-UHD4K-60-422 | 3840x2160 | 60 | 4:2:2 | 10 | ✓ | \checkmark |
| | IPX-TICO-UHD4K-120-422 | 3840x2160 | 120 | 4:2:2 | 10 | √ | \checkmark |
| | IPX-TICO-UHD4K-180-422 | 3840x2160 | 180 | 4:2:2 | 10 | / | \checkmark |
| | IPX-TICO-UHD4K-60-444 | 4096x2160 | 60 | 4:2:2 / 4:4:4 | 8, 10, 12, 16 | \checkmark | \checkmark |
| | IPX-TICO-UHD4K-120-444 | 4096x2160 | 120 | 4:2:2 / 4:4:4 | 8, 10, 12, 16 | / | \checkmark |
| HDTV2/8K | IPX-TICO-UHD8K-60-422 | 7680x4320 | 60 | 4:2:2 | 10 | / | \checkmark |
| | IPX-TICO-UHD8K-120-444 | 7680x4320 | 120 | 4:4:4 | 10 | / | ✓* |

*Available in pre-order only.

CONTACT INTOPIX FOR YOUR OWN CUSTOM IP-CORE CONFIGURATION

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